Application Note

PWM Amplifier Output Power Calculator

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1. INTRODUCTION

The PWM amplifier output power calculator is used to determine the effective root mean square (rms) power for a given speaker load. The spreadsheet is configured to calculate the actual power delivered to the speaker load for three typical speaker-load configurations, half-bridge tied, full-bridge tied and parallel full-bridge tied. To access the spreadsheet, click on this link: http://www.cirrus.com/en/support/AN268. The PWM Amplifier Output Calculator is available in two forms. If a version of Microsoft® Excel is available on your local computer, then download the Excel spreadsheet version of the power output calculator. If not, then use the interactive power calculator located at the above web site.

2. AMPLIFIER OUTPUT CONFIGURATIONS

2.1 Half-Bridge

Half-bridge tied speaker loads are driven on a single side by the PWM output, with the other side of the load referenced to ground, see Figure 1. For single voltage rail systems with a voltage of VP, the amplifier output will contain a DC voltage offset equal to VP divided by 2 that must be blocked from the speaker load. This is generally accomplished by using a large electrolytic capacitor (C) in series with the output following the 2-pole LC filter used to attenuate the PWM switching frequency. The electrolytic capacitor is usually polarized and care must be take to wire the "+" terminal of the capacitor towards the output of the PWM output. For proper operation and increased circuit reliability, the maximum ripple current specification for the capacitor must be larger than the peak-to-peak current to the speaker load.

The capacitor (C) along with the speaker load (R), which is generally in the 4 ohm or less range for this configuration, form a high pass filter. The -3dB corner frequency is determined by the equation Fs = 1/(6.28*R*C). The particular speaker load supported and the desired corner frequency determines the size of the capacitor measured in microfarads.

To avoid loud pops in the speaker caused by the instantaneous voltage across the DC blocking capacitor at the beginning of the power on sequence, a voltage ramp up sequence should be used, such as the Ramp-up feature of the CS44800/44600. This feature will quickly bring the output of the PWM amplifier to the half rail voltage of VP divided by 2 in a linear fashion without causing any loud pops.

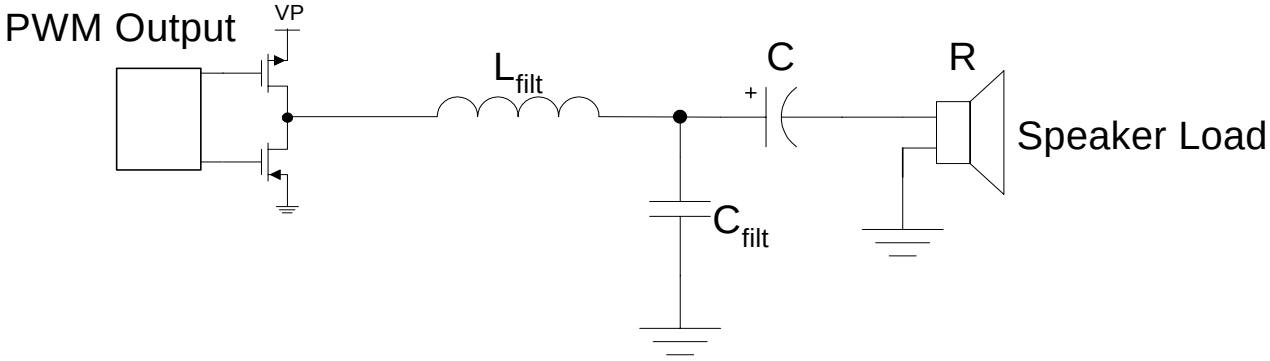

Figure 1. Half-Bridge Output Configuration

2.2 Full-Bridge

With using the same VP voltage rail level as with the half-bridge configuration above, increased power to the speaker load is accomplished by using a pair of PWM outputs providing a differential signal to drive a full-bridge tied speaker load, see Figure 2. In this configuration, the speaker load is not referenced to ground and is continuously driven by both the "+PWM Output" and "-PWM Output" signals from the amplifier. This effectively doubles the voltage across the load resulting in a quadrupling of the output power since the power is a function of the square of the voltage.

With full-bridge configurations, care must be taken not to exceed the maximum current specification limits for the components. This is accomplished by increasing the minimum speaker load over what was driven for the half-bridge example above (to 8 ohms versus 4 ohms). Since the power out is inversely proportional to the resistive speaker load, then instead of quadrupling the power output, now the power output is double and thereby lowering the maximum output current. Even though there are two L_{filt} components in series for the full-bridge configuration, the value for this inductor remains the same as for the half-bridge configuration since the speaker load is now doubled.

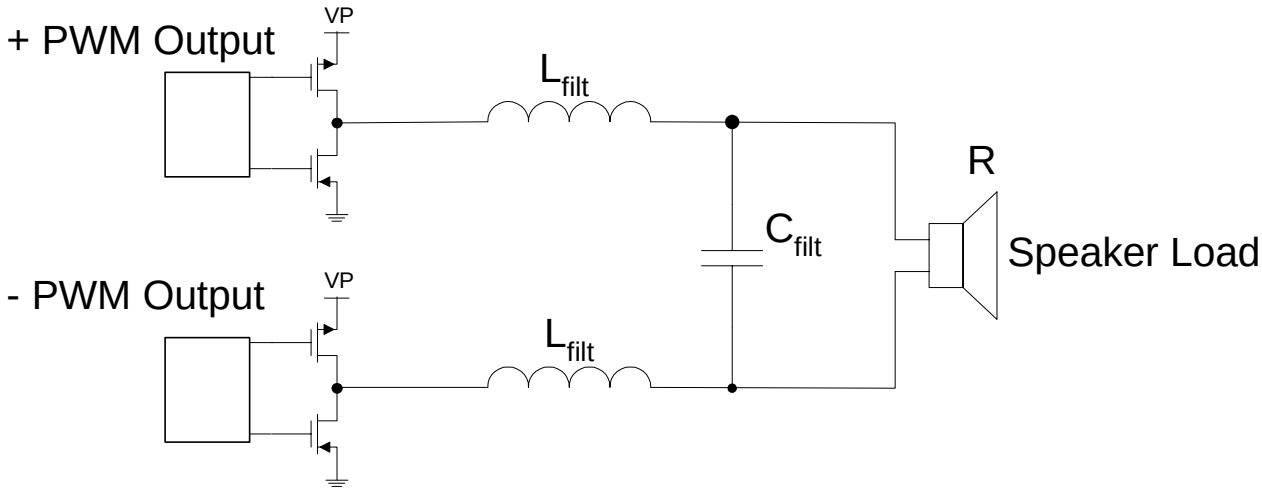

Figure 2. Full-Bridge Output Configuration

2.3 Parallel Full-Bridge

Parallel full-bridge tied loads are driven differentially similar to full-bridge tied loads, but can deliver more current to the speaker load, with more efficiency, see Figure 3. Multiple PWM outputs are tied together in a parallel fashion which effectively causes the Rds_on of these switches to also be in parallel, thereby dividing the Rds_on as seen by the load current by a factor of 2. The benefit of doubling VP to the load is maintained and the current carrying capability is also doubled, allowing smaller speaker loads to be supported. This configuration is typically used when higher power levels are required such as when driving a subwoofer channel.

Since smaller speaker loads of 4 ohms or less, similar to the half-bridge output topology, are allowed to be driven in this configuration, the value for L_{filt} must be halved to maintain a comparable LC filter response to the half-bridge and full-bridge configurations. Also note that the parallel full-bridge configuration should only be attempted with power stage devices which integrate all MOSFET devices in a single package. In this case, the characteristics for each MOSFET switch are highly correlated and matched to the other MOSFET switches such as to avoid cross-conduction currents and high levels of distortion due to switching errors.

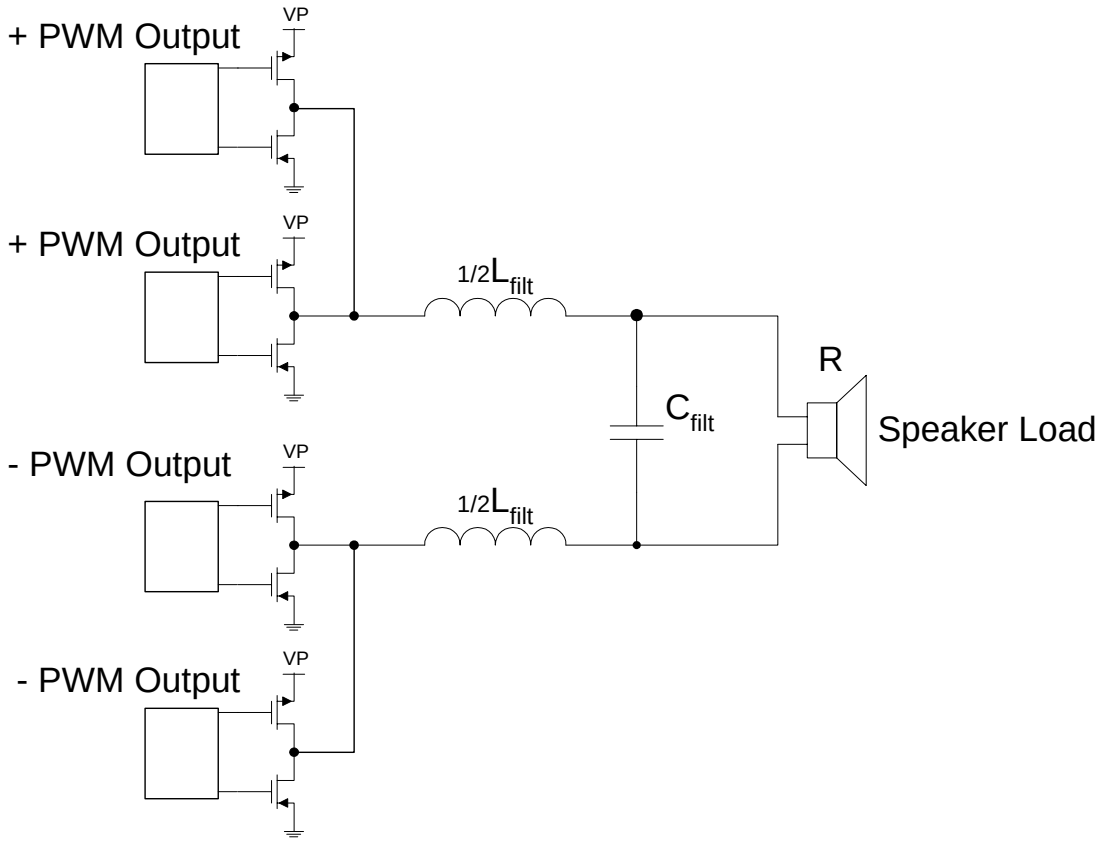

Figure 3. Parallel Full-Bridge Output Configuration

2.4 Power Calculations

A view of the downloaded spreadsheet is shown below. To modify the Assumptions or the Speaker Load in the calculations, double-click any cell with blue text within the spreadsheet. All parameters shown in blue can be modified with specific system or device parameters.

The Voltage Rail VP is the power supply nominal DC output expressed in volts. This value is taken at the input pin of the PWM power device.

The modulation index is the amount of full-scale signal that can be output from the PWM amplifier. This value is usually below 0.95 and is determined by both the modulator effectiveness and the ability of the PWM output power stage to handle small input pulse widths.

The PWM output Rds_on is the nominal series resistance of the MOSFET device as specified by the manufacture. As the temperature of the power device rises, so will this value.

The inductor resistance is the resistance value of the inductor at DC. This value is specified by the inductor manufacture and should be as low as possible. Typical values are between 0.05 and 0.15 ohms.

The capacitor's Equivalent Series Resistance (ESR) is specified by the component manufacturer. The capacitor ESR is only used in the half-bridge configurations when a capacitor is required to block any DC offset.

The "Power Out" calculation is the total power output for the specified channel. This is not the power delivered to the speaker load. The "Power Out" formula is: Power out = $(Vrms)^2/Rtotal$, where Vrms is the root mean square of the VP voltage rail multiplied by the modulation index. Rtotal is the sum of all the resistances along the amplifier

output path. In addition to the speaker load, these include the resistance of all the MOSFETs and filter inductors. Substituting gives:

Power out = (VP * Mod. Index/2.83)^2 / (Spkr Load + PWM Rds_on + Ind. Resistance).

The 2.83 value in the denominator converts the DC value of VP to an RMS value. For half-bridge configurations, the ESR of the capacitor is also added to the total resistance.

For full-bridge amplifier outputs, the current flow will actually incur the PWM Rds_on and the Inductor Resistance twice as it flows from one PWM output, through the load, and into the other PWM output. Because of the additional impedance, this configuration is a little less efficient than the others.

The parallel full-bridge amplifier is not only capable of supplying more current, it is more efficient than the full-bridge configuration. The reason is that since the two PWM outputs are in parallel, then the PWM Rds_on resistance of each output is also in parallel. This effectively cuts the total PWM Rds_on in half.

To calculate the actual power delivered to the speaker load, the "Total current" is calculated. The actual "Power at the load" is then the square of the "Total current" multiplied times the speaker load. This power level is somewhat lower than the "Power out" calculation due to the other resistive losses within the circuit. The 0.1% THD+N power number is the typical full scale, non-clipping output power at the load. The 1% THD+N power value represents a small amount of clipping when the output of the PWM modulator is brought above full scale and is approximately the 0.1% power output multiplied by 1.15. To approximate the generally specified 10% THD+N power value given by many amplifier manufacturers, multiply the 0.1% THD+N power output value by 1.75.

The "Power dissipation per channel" is the amount of power that will be dissipated within the MOSFETs for a single channel. The calculation is simply the square of the "Total current" multiplied by the PWM Rds_on for that channel. For bridge-tied channels, the effective PWM Rds_on is double that for a half-bridge channel. This increases the overall power dissipation for a channel which is configured for full-bridge operation. If multiple channels are contained within a single power output stage module, then the total power dissipation for all channels must be summed in order to calculate proper cooling requirements.

Assumptions	
Voltage Rail Vp (volts)	35
Modulation Index	0.87
PWM Output Rds_on (ohms)	0.25
Capacitor ESR (ohms)	0.05
Inductor Resistance (ohms)	0.05

Calculations

	Half-Bridged Tied			Full-Bridge Tied			Parallel Full-Bridge Tied		
Speaker Load (ohms)	8	6	4	8	6	4	8	6	4
Power out (W)	13.86	18.23	26.61	53.85	70.16	100.67	55.46	72.93	106.46
Total current (rms)	1.29	1.69	2.47	2.50	3.26	4.68	2.58	3.39	4.95
Total current (peak)	1.82	2.40	3.50	3.54	4.61	6.61	3.64	4.79	7.00
Power at the Load (W)									
0.1% THD+N	13.28	17.23	24.47	50.09	63.79	87.54	53.13	68.91	97.89
1% THD+N (x1.15)	15.28	19.81	28.14	57.60	73.35	100.67	61.10	79.24	112.57
10% THD+N (x1.75)	23.25	30.15	42.83	87.66	111.63	153.19	92.99	120.59	171.31
Effciency	0.96	0.94	0.92	0.93	0.91	0.87	0.96	0.94	0.92
Power Dissipation (W) per channel	0.42	0.72	1.53	3.13	5.32	10.94	1.66	2.87	6.12

3. REVISION HISTORY

Release	Date	Changes
Rev 1	May 2005	1st Preliminary Release

Table 1. Revision History